What is claimed is:

1. An apparatus, comprising:

- a clock source to generate a clock signal;

- a first circuit, coupled to a first supply voltage source, to generate a first data signal and a second circuit coupled to a second supply voltage source;

- a first level shifter, coupled to the first circuit, to generate a level shifted data signal in response to the first data signal; and

- a downstream latch, having a pair of inputs coupled to the first level shifter and the clock source and an output coupled to the second circuit, to generate an output data signal in response to the level shifted data signal and the clock signal.

2. The apparatus according to claim 1, further comprising:

- a second level shifter, coupled between the clock source and the downstream latch, to generate a level shifted clock signal in response to the clock signal; and

- the downstream latch, having the pair of inputs coupled to the first level shifter and the second level shifter, to generate the output data signal in response to the level shifted data signal and the level shifted clock signal.

3. The apparatus according to claim 2, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch has an open and a close state; and the downstream latch is switched from the close state to open state by a triggering clock edge selected from the rising clock edge and the falling clock edge.

4. The apparatus according to claim 2, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch has an open and a close state; and the downstream latch is switched from the close state to open state by a triggering clock edge selected from the rising clock edge and the falling clock edge and switched

from the open state to a close state by the non-selected clock edge of the rising clock edge and the falling clock edge.

5. The apparatus according to claim 3, further comprising:

- a delay element coupled between the clock source and the second level shifter and responsive to the clock signal to provide a delayed clock signal to the second level shifter.

6. The apparatus according to claim 5, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay the triggering clock edge until after an arrival of the rising and falling data edges at the second level shifter.

7. The apparatus according to claim 5, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched.

8. The apparatus according to claim 6, further comprising:

- a flip-flop, coupled to the first circuit, including a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifted, to generate the first data signal; and wherein the downstream latch is a downstream slave latch.

9. The apparatus according to claim 8, wherein the first circuit generates an input signal; the master latch has an input to receive the input signal; and the flip-flop is operable to generate the first data signal in response to the input signal.

10. An apparatus, comprising:

- a microprocessor including a central processing unit (CPU) section having a

first supply voltage source; an input-output (I/O) section having a second supply voltage source; a clock source to generate a clock signal; and a selected section of the CPU section and the I/O sections being operable to generate a first data signal;

- a converter circuit including a first level shifter, coupled to the selected section, to generate a level shifted data signal in response to the first data signal; a second level shifter, coupled to the clock source, to generate a level shifted clock signal in response to the clock signal; and a downstream latch, having a pair of inputs coupled to the first and second level shifters and an output coupled to the non-selected section of the CPU and I/O sections, to generate an output data signal in response to the level shifted data signal and level shifted clock signal.

11. The apparatus according to claim 10, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch has an open and a close state; and the downstream latch is switched from the close state to open state by a triggering clock edge selected from the rising clock edge and the falling clock edge.

12. The apparatus according to claim 11, further comprising:

- a delay element coupled between the clock source and the second level shifter and responsive to the clock signal to provide a delayed clock signal to the second level shifter.

13. The apparatus according to claim 12, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay the triggering clock edge until after an arrival of the rising and falling data edges at the second level shifter.

14. The apparatus according to claim 13, wherein the converter circuit includes a flip-flop having a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output

coupled to the first level shifted, to generate the first data signal; and the downstream latch being a downstream slave latch.

15. The apparatus according to claim 14, wherein the selected section generates an input signal; the master latch has an input to receive the input signal; and the flip-flop is operable to generate the first data signal in response to the input signal.

16. A system, comprising:

- a microprocessor including a central processing unit (CPU) section coupled to a first supply voltage source; an input-output (I/O) section coupled to a second supply voltage source; a clock source to generate a clock signal; and the CPU section being operable to generate a first data signal;

- a converter circuit including a first level shifter, coupled to the CPU section, to generate a level shifted data signal in response to the first data signal; a second level shifter, coupled to the clock source, to generate a level shifted clock signal in response to the clock signal; and a downstream latch, having a pair of inputs coupled to the first and second level shifters and an output coupled to the I/O section, to generate an output data signal in response to the level shifted data signal and level shifted clock signal;

- a source synchronous bus, coupled to the I/O section, to receive the level shifted data signal and the level shifted clock signal; and

- an I/O module coupled to the source synchronous bus.

17. The system according to claim 16, wherein the I/O module is a selected one of a graphics and a video controller.

18. The system according to claim 16, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch has an open and a close state; and the downstream latch is switched from the close state to open state by a triggering clock

edge selected from the rising clock edge and the falling clock edge.

19. The system according to claim 18, further comprising:

- a delay element coupled between the clock source and the second level shifter and responsive to the clock signal to provide a delayed clock signal to the second level shifter.

20. The system according to claim 19, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay the triggering clock edge until after an arrival of the rising and falling data edges at the second level shifter.

21. The system according to claim 20, wherein the converter circuit includes a flip-flop having a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifted, to generate the first data signal; and the downstream latch being a downstream slave latch.

22. The system according to claim 21, wherein the CPU section generates an input signal; the master latch has an input to receive the input signal; and the flip-flop is operable to generate the first data signal in response to the input signal.

23. A method, comprising:

- supplying a first supply voltage, a second supply voltage, and a clock signal having a rising clock edge and a falling clock edge;
- shifting a first data signal from the first supply voltage to the second supply voltage by way of a first level shifter;
- generating a level shifted data signal from the first level shifter with the level shifted data signal having a plurality of rising and falling data edges that are mismatched; and

- latching the level shifted signal in response to one of the rising and falling clock edges after the rising and falling data edges have occurred.

24. The method according to claim 23, wherein latching the level shifted data signal includes using a downstream latch to latch the level shifted data signal after the rising and falling data edges have reached the latch.

25. The method according to claim 24, further comprising:

- shifting the clock signal from the first supply voltage to the second supply voltage by way of a second level shifter to generate a level shifted clock signal having the rising clock edge and the falling clock edge.

26. The method according to claim 25, further comprising:

- delaying the clock signal by a predetermined amount exceeding a period of time during which the plurality of rising and falling data edges are mismatched.

27. The method according to claim 26, further comprising:

- delaying an input signal by a single clock cycle of the clock signal with a flip-flop having a master latch and a slave latch to generate a delayed input signal; and

- providing the delayed input signal to the first level shifter.